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DAC4

Technical Design Document

Contents:

Document Revision 1.4

This Document applies to Board Revision B

1. Introduction

This DAC is my fourth DAC project since 1993. In the past I made some important experiences especially with the DAC3 project where I could sonically evaluate different DAC chips under the same condition. I found that Sigma-Delta-Converters are very close to multi-bit designs. Their advantage is the simple implementation and the possibility of using a simple output stage design together with a short signal path. With the appearance of the next generation of 24/96 Sigma-Delta-Converters from Analog Devices, Burr Brown and Crystal I decided to dedicate my next DAC project to this generation of Sigma-Delta-DAC-chips exclusively.

I also decided to design a new main board for modules which can host a variety of the next generation of combined Digital-Input-Receiver/Sample-Rate-Converters chips from Analog Devices and Crystal. These chips have an inherent jitter reduction because the sample-rate-converter effectively acts as a low-pass filter for jitter.

Today all modern chips come in small SOIC and even smaller SSOP packages. Both DIR and DAC modules are therefore relatively tiny (40,5 x 20,5mm) compared to DAC3-Modules.

2. Features

- Plug-in modules for Digital-Input-Receiver and Digital/Analog-Converters (32 pins, 40,5 x 20,5mm)
- Inherent jitter reduction through sample rate converter
- Digital-Input-Receiver / Sample-Rate-Converter modules based on Analog Devices® AD1892 or Crystal® CS8420
- Standard Digital-Input-Receiver Crystal® CS8415A
- Sigma-Delta DAC modules based on Analog Devices® AD1855/AD1854/AD1853/AD1852, Crystal® CS4390/CS4396/CS4397, or Burr Brown® PCM1716, PCM1732, PCM1739
- 2^{nd}-order passive low-pass filter
- Balanced output stage using a single discrete operational amplifier module
- 3 separate power supplies delivering 7 independently regulated voltages

3. Specifications

Table 1: DAC4 Specifications

SPDIF Digital Input	75ohms
Input Sample Rate	32kHz to 96kHz *
DAC Sample Rate	48kHz or 96kHz *
Input Word Width	16 to 24bit
Signal Path Width	24bit
Output Impedance	390ohms
Analog Output	2,0/4,0V RMS (single ended/balanced) **
Recommended Load Impedance	>= 22kohms
Board Size	210.8mm x 179.1mm

* Depending on DIR module used
** Depending on DAC module used

4. Main Board

Digital Inputs

The DAC4 main board is designed to have two input facilities that can be selected using jumper JP2 (see table 4 below):

1. Standard SPDIF serial port (75ohms input impedance)
2. Two-phase AES3 serial port (TTL level) using the control bus interface

The SPDIF port may be used in cases where only one input is required e. g. when the DAC is dedicated to a single source (CD-player). If more than one input is required an input-switching device connected to the DAC's control bus is necessary.

Control Bus

The control bus is primarily designed to:

1. Control DIR and DAC chips by software using a micro-controller as SPI-master device
2. Extend the input capacity of the DAC
3. Connect a display unit to indicate the status of the system

Table 2: Control Bus Pin Description

Pin #	Mnemonic	Direction *	Description
1	CLE1	I	SPI bus latch enable for device #1 (DAC) **
2	CLE0	I	SPI bus latch enable for device #0 (DIR) **
3	INT	O	Interrupt signal from device #0 (DIR)
4	F2	O	DAC sample frequency bit 2 (see Table 3) ***
5	F1	O	DAC sample frequency bit 1 (see Table 3) ***
6	F0	O	DAC sample frequency bit 0 (see Table 3) ***
7	OSCD	I	Oscillator disable signal (active low, open collector)
8	VD+	PWR	+13V digital power supply
9	RXP	I	Positive phase AES3 data input
10	RXN	I	Negative phase AES3 data input
11	DGND0	PWR	Digital ground
12	DGND1	PWR	Digital ground
13	DGND2	PWR	Digital ground
14	RESET	O	Reset signal (active low)
15	DEEMP	O	De-emphasis indicator signal
16	ERROR	O	DIR error signal (no lock, receive data error)
17	HDCD	O	HDCD protocol detection signal
18	CDI	I	SPI bus data input **
19	CDO	O	SPI bus data output **
20	CCLK	I	SPI bus clock **

* Direction indicated from main board's perspective.
** Refer to individual data sheet for timing issues
*** Due to SRC the DAC sample frequency may differ from input sample frequency.

Table 3: Control Bus Sample Frequency Decoding

F2	F1	F0	Sample Frequency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	96 kHz
1	0	0	88.2 kHz
1	0	1	48 kHz
1	1	0	44.1 kHz
1	1	1	32 kHz

Jumper Settings

Jumper block JP1 is divided into two sections:

1. Selection of DAC sample frequency according to crystal frequency
2. Selection of digital-input-receiver options (See individual module section in chapter 6.)

Table 4: Jumper Settings JP1

1-2	3-4	5-6	DAC Sample Frequency	Crystal Frequency
off	off	off		Oscillator not used *
off	on	on	96 kHz	24,576 MHz **
on	off	on	48 kHz	24,576 MHz **
on	off	off	88.2 kHz	22,5792 MHz
on	on	off	44.1 kHz	22,5792 MHz

* Use this setting with non-SRC DIR chips (e. g. CS8415A)
** Standard crystal

Jumper block JP2 is used to set-up the desired digital input:

Table 5: Jumper Settings JP2

1-2	3-4	Input
on	on	On board SPDIF serial port
off	off	Control bus interface

Crystal Oscillator

After trying several oscillator types (series and parallel resonant circuits) I found that none of them did work properly with the crystals available. Therefore I started looking for high quality integrated crystal oscillators. After trying several models I found that low-jitter integrated crystal oscillator manufactured by Fox Electronics® (JITO-2 series) brought the best results by far. The standard oscillator frequency is 24,576MHz but other frequencies (e. g. 25,000MHz) can also be used.

Filter and Output Stage

The major design goal for the filter and output stage was to keep the overall circuit as simple as possible and not to use any positive feedback filters.
My experience from the DAC1 and DAC3 designs is that the filter should be passive and not higher as of second order. For non-noise-shaping converters (multi-bit converters) a first order filter should be sufficient especially if using tube equipment that acts as a low-pass filter too.
The solution is to place a passive low-pass filter before and a second one after a gain stage to build a second order passive low-pass filter with a slow roll off (-3db @ 49,5kHz). To keep the output impedance of the whole circuit in a reasonable range the resistor of the second low-pass has been set to 390ohms.

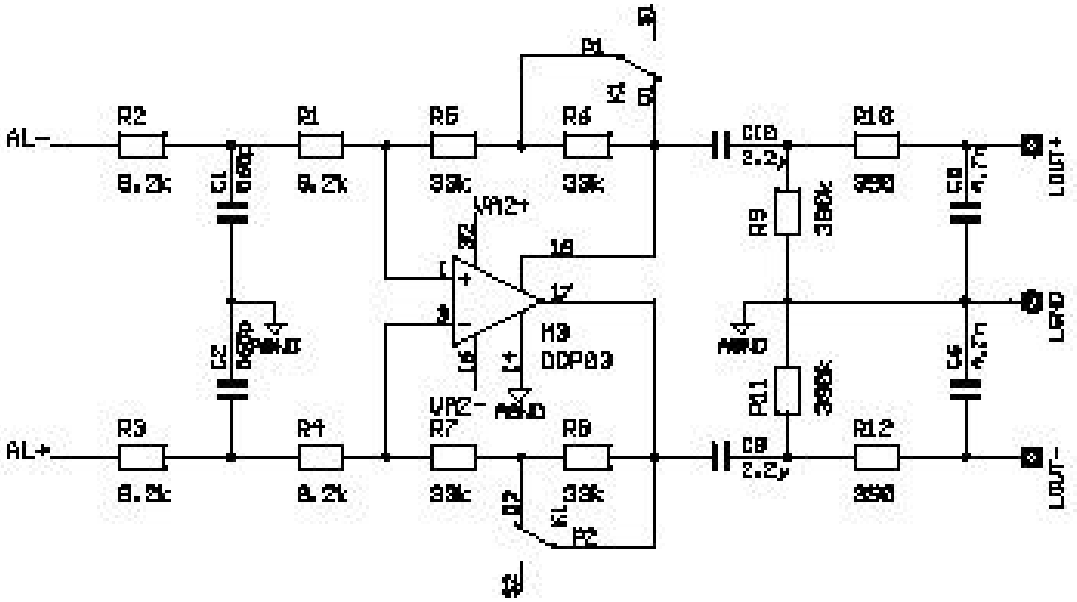

Fig. 1: Schematic of Filter and Output Stage

The gain of the output stage is switch-able via a relay circuit from +6 to +12db to support gain adjustment when playing HDCD encoded source material on a HDCD compatible DAC (e. g. Burr Brown PCM1732).
The output capacitors (2,2µF) probably may be substituted by a piece of wire but this really depends on the stability and value of the offset voltage from the DAC-chips.
I didn't want to build a DC-servo device to get rid of these coupling capacitors because this increases the feedback applied in the low frequency range drastically in order of the open loop gain of the operational amplifier used to build the servo loop. This is absolutely not desirable because it would mean to have 158db feedback in the low frequency range and 58dB feedback above 50Hz.
In general I think high quality capacitors are a better solution than using servo-loops that are introducing an unequal amount of feedback over the frequency range.

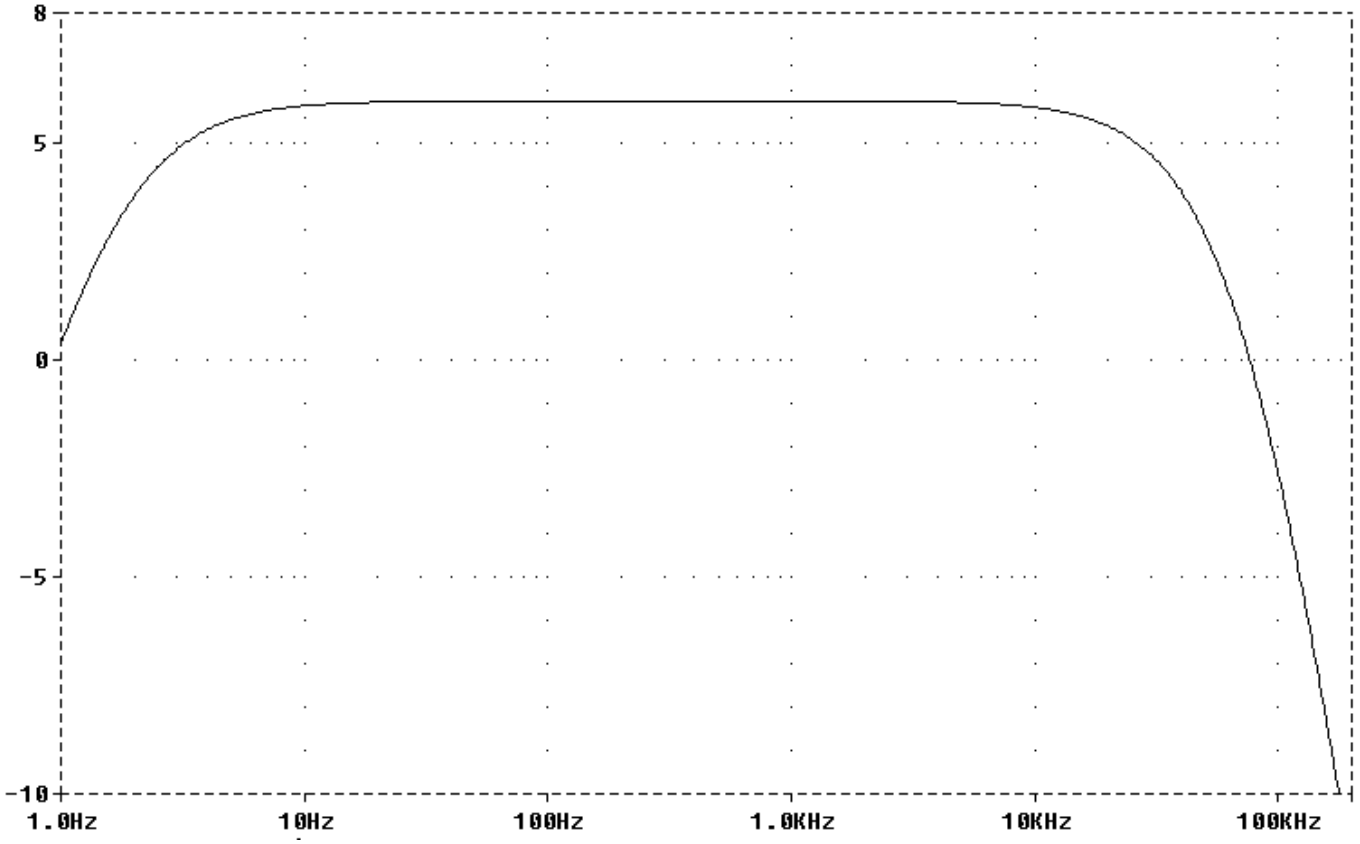

Fig. 2: Frequency Response of Filter and Output Stage (simulated)

Digital Power Supplies

All power supply circuits are built as a cascade of two regulators. For the digital power supplies the first regulator using a LM317 delivers 13,0V to three other dedicated LM7805s, which supply 5,0V to:

1. the crystal oscillator and reset pulse generator
2. the digital part of the DIR module
3. the digital part of the DAC module

The LM317 also directly supplies the control bus with 13,0V. There are only very few power supply bypass capacitors on the main board because each module comes with its own set of SMD-capacitors being mounted as close as possible to the power supply pins of the chip.

Analog Power Supplies

The analog power supplies are also built as a cascade of two regulators.

The first regulator stage is LM317/337 based delivering +/-26V. The second regulator stage is build around an integrated operational amplifier CA3140 controlling a high-speed Darlington transistor.
The CA3140 has been selected because it is able to work properly even when the input voltages are close to the supply voltages. Second reason is the possibility to influence the dynamic behavior of the amplifier through external compensation capacitors. The reference voltage is delivered by two LM78L15/79L15 devices and split down by two resistors. Hence the regulator works entirely in its linear region.
There is a second set of regulators to supply +5V to the analog part of the DIR and the DAC chips. This regulator works exactly as described above.

Common to all power supplies is the usage of "audiophile-style" rectifiers. These devices are designed to meet the sonic characteristics of rectifier valves (WE274, 5U4G, EZ34, EZ81, etc.) as close as possible.
To achieve this goal one has to get rid of the noise caused by the high current peaks resulting from charging the electrolytic capacitors. This is achieved with using high-speed rectifier diodes, a small capacitor parallel to each diode and a resistor in series with each to reduce the current peak and to match the impedance to the following stage.

5. Operational Amplifier Module DOP03

Specifications

Table 6: DOP03 Specifications

Open-loop gain	64dB (balanced)
Open-loop bandwidth	50kHz *
Input impedance	10^{12}ohms
Voltage output	Min. 9V RMS
Current output	Min. 3mA RMS
Power supply	+/-15V

* uncompensated

Circuit Description

The gain stage in between the two passive filters is a two-stage differential amplifier with emitter-follower buffered balanced outputs. The current in the first stage is stabilized by an adjustable current source. Such an operational amplifier is not commercially available as an integrated circuit. Therefore I created a new type of module that has the same size as the DIR and DAC modules used for DAC4.

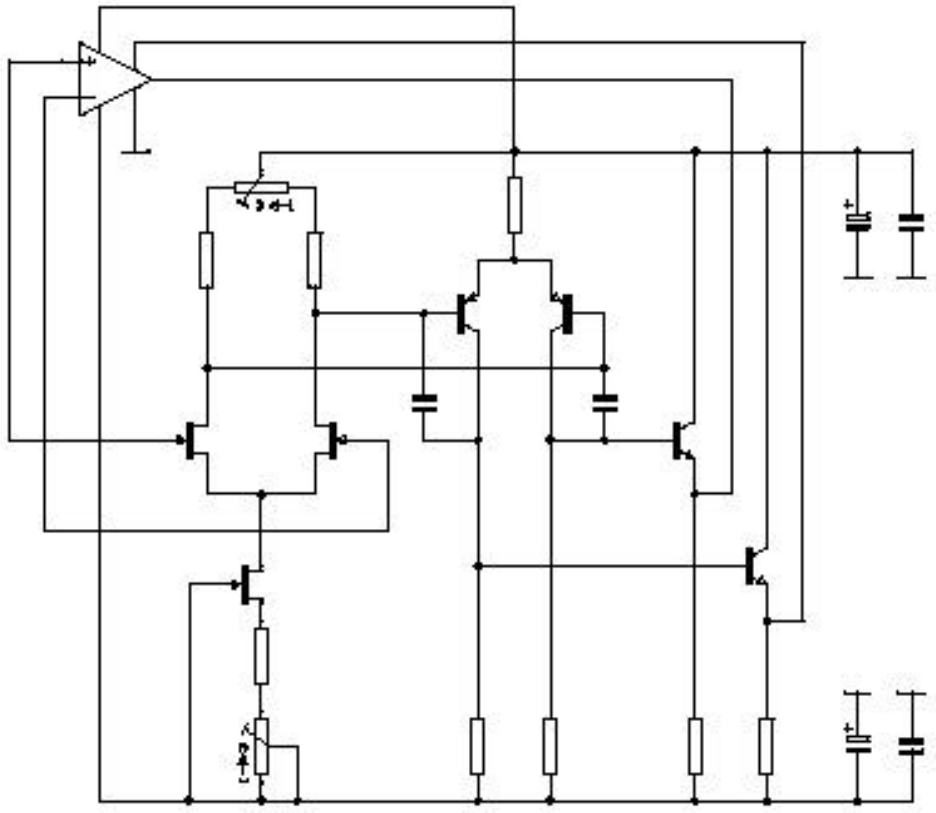

Fig. 3: Schematic of discrete bi-phase operational Amplifier Module DOP03

The discrete bi-phase operational amplifier module DOP03 makes it possible to implement all features wanted. As the two transistor pairs of the two differential stages need to be matched to a high extend it is preferable for the builder of a DAC4 to purchase these modules ready-built and adjusted. The cost for an individual to buy at least 50 transistors of each type and the equipment to find two really good pairs would probably be much higher as the cost of the finished module.
Therefore DOP03 modules will only be available ready-built and adjusted. I also will not publish any details like part values or type of transistors used.

6. Digital Input Receiver Modules

Common Specifications

Table 7: DIR Module Pin Description

Pin #	Mnemonic	Direction *	Description
1	VD+	PWR	Digital section power supply +5V
2	F0	I/O	DAC sample frequency bit 0 (see Table 3) **
3	F1	I/O	DAC sample frequency bit 1 (see Table 3) **
4	F2	I/O	DAC sample frequency bit 2 (see Table 3) **
5	S0	I	Option select bit 0 ***
6	S1	I	Option select bit 1 ***
7	S2	I	Option select bit 2 ***
8	NC1		
9	RXP	I	Positive phase AES3 data input
10	RXN	I	Negative phase AES3 data input
11	RESET	I	Reset signal (active low)
12	NC2		
13	CLK/2	I	Oscillator low frequency clock (1/2)
14	CLK	I	Oscillator high frequency clock
15	NC3		
16	DGND	PWR	Digital section ground
17	AGND	PWR	Analog section ground
18	NC4		
19	SDATA	O	Serial audio data
20	SCLK	O	Serial audio data bit clock
21	LRCLK	O	Serial audio data left/right clock
22	MCLK	O	Master clock
23	OSCD	O	Oscillator disable signal (active low, open collector)
24	ERROR	O	Error signal (no lock, receive data error)
25	DEEMP	O	De-emphasis indicator signal
26	VA+	PWR	Analog section power supply +5V
27	NC5		
28	INT	O	Interrupt signal
29	CDO	O	SPI bus data output ****
30	CDI	I	SPI bus data input ****
31	CCLK	I	SPI bus clock ****
32	CLE	I	SPI bus latch enable ****

* Direction indicated from module's perspective.
** Due to SRC the DAC sample frequency may differ from input sample frequency.
*** Refer to jumper settings in the individual module description
**** Refer to individual data sheet for timing issues.

Individual Specifications

Table 8: DIR Modules individual Specifications

	AD1892	**CS8420**	**CS8415A**
Includes Sample-Rate-Converter	Yes	Yes	No
Maximum Input Sample Rate	48kHz	96kHz	96kHz
Maximum Output Sample Rate	48kHz	96kHz	96kHz
Maximum Input Word Width	20bit	24bit	24bit
Signal Path Width	20bit	24bit	24bit
Output Data Format	I^2S	I^2S	I^2S
Digital Filter Passband Ripple	+/- 0,015dB	+/- 0,0007dB	n. a.
Digital Filter Stopband Attenuation	110dB	110dB	n. a.
Digital Power Supply	+5V	+5V	+5V
Analog Power Supply	n. a.	+5V	+5V

Table 9: Jumper Settings JP1 for AD1892 DIR Module

7-8	**9-10**	**11-12**	**DAC Master Clock Frequency**
		off	12,288MHz *
		on	24,576MHz *

* When using standard 24,576MHz crystal

7. Digital/Analog Converter Modules

Common Specifications

Table 10: DAC Module Pin Description

Pin #	Mnemonic	Direction *	Description
1	VD+	PWR	Digital section power supply +5V
2	NC1		
3	F0	I	DAC sample frequency bit 0 (see Table 3) **
4	F1	I	DAC sample frequency bit 1 (see Table 3) **
5	F2	I	DAC sample frequency bit 2 (see Table 3) **
6	NC2		
7	RESET	I	Reset signal (active low)
8	DEEMP	I	De-emphasis enable signal
9	ERROR	I	Mute on error signal
10	NC3		
11	MCLK	I	Master clock
12	LRCLK	I	Serial audio data left/right clock
13	SCLK	I	Serial audio data bit clock
14	SDATA	I	Serial audio data
15	NC4		
16	DGND	PWR	Digital section ground
17	AGND	PWR	Analog section ground
18	VA2-	PWR	Analog section power supply -15V
19	AOUTR-	O	Negative phase right audio output
20	AOUTR+	O	Positive phase right audio output
21	NC5		
22	AOUTL-	O	Negative phase left audio output
23	AOUTL+	O	Positive phase left audio output
24	VA2+	PWR	Analog section power supply +15V
25	VA1+	PWR	Analog section power supply +5V
26	NC6		
27	GAIN	O	+6dB gain in analog stage signal
28	HDCD	O	HDCD protocol detection signal
29	NC7		
30	CDATA	I	SPI bus data input ***
31	CCLK	I	SPI bus clock ***
32	CLE	I	SPI bus latch enable ***

* Direction indicated from module's perspective.
** Due to SRC the DAC sample frequency may differ from input sample frequency.
*** Refer to individual data sheet for timing issues.

Individual Specifications

Table 11: DAC Modules individual Specifications

	AD1855	**AD1854**	**AD1853**	**AD1852**	**CS4390**	**CS4396 CS4397**	**PCM1716 PCM1728**	**PCM1732**	**PCM1737 PCM1739**
DAC Type	Multi-Bit PWM	Multi-Bit PWM	Multi-Bit PWM	Multi-Bit PWM	Single-Bit PWM	Multi-Bit PWM	Multi-Bit PWM	Multi-Bit PWM	Multi-Bit PWM
Maximum Input Sample Rate	96kHz	96kHz	192kHz *	192kHz *	48kHz	192kHz *	96kHz	96kHz	192kHz *
Maximum Input Word Width	24bit	24bit	24bit	24bit	24bit	24bit	24bit	24bit	24bit
Resolution claimed	20bit	20bit	24bit	24bit	24bit	24bit	24bit	24bit	24bit
Input Data Format	I^2S	I^2S	I^2S	I^2S	I^2S	I^2S	I^2S	I^2S	I^2S
Signal-to-Noise-Ratio (A-weighted)	113dB	112dB	114dB	116dB	115dB		103dB	103dB	104dB
Dynamic Range (A-weighted)	110dB	113dB	113dB	115dB	106dB	120dB	103dB	103dB	105dB
THD+Noise	-97dB	-101dB	-104dB	-104dB	-98dB	-100dB	-97dB	-96dB	-100dB
Master Clock Frequency	256 * fs	256 * fs	256/512 * fs	256/512 * fs	256/512 * fs	256/512 * fs	256/512 * fs	256/512 * fs	256/512 * fs
Digital Filter Passband Ripple	+/- 0,04dB	+/- 0,04dB	+/- 0,0005 dB	+/- 0,0005 dB	+/- 0,001dB	+/- 0,0001 dB	+/- 0,002dB	+/- 0,0001 dB	+/- 0,002dB
Digital Filter Stopband Attenuation	47dB	47dB	115dB	115dB	75dB	102dB	82dB	132dB	82dB
Analog Output Voltage	2,0V RMS	2,0V RMS	2,0V RMS	2,0V RMS	2,0V RMS	2,0V RMS	2,2V RMS	2,0V RMS	2,2V RMS
Analog Output Type	Balanced	Balanced	Balanced	Balanced	Balanced	Balanced	Single ended	Balanced	Single ended
Digital Power Supply	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V
Analog Power Supply	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V +/-15V	+5V

* The SPDIF input format only supports a maximum of 96kHz

8. Reference

Recommended Reading

- John Watkinson - The Art of Digital Audio
- Howard Johnson, Martin Graham - High Speed Digital Design: A Handbook of black Magic
- Data sheets of the DIR and DAC modules used in the version of DAC4 you are going to build

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